CLAIMS

What is claimed is:

1. A method for producing non-warped semiconductor die from a wafer having a frontside, a backside, and a frontside layer on a portion of said semiconductor wafer causing a stress, said method comprising:

reducing a cross-section of said semiconductor die by thinning the semiconductor die;
applying a stress-balancing layer to said; and
singulating said wafer into a plurality of semiconductor die.

2. A method in accordance with claim 1, wherein said frontside layer comprises a layer applied in fabrication of said semiconductor die.

3. A method in accordance with claim 1, wherein said frontside layer comprises a layer of passivation material.

4. A method in accordance with claim 1, wherein said thinning comprises grinding.

5. A method in accordance with claim 1, wherein said thinning comprises a chemical-mechanical method.

6. A method in accordance with claim 1, wherein said semiconductor die comprises an integrated circuit semiconductor die.

7. A method in accordance with claim 1, wherein said stress-balancing layer comprises a layer substantially covering said backside.

8. A method in accordance with claim 1, wherein said stress-balancing layer comprises a strip covering a selected portion of a row of semiconductor dice on said wafer.

9. A method in accordance with claim 1, wherein said stress-balancing layer comprises a plurality of portions, each said portion covering a selected portion of the thinned semiconductor die on said wafer.

10. A method in accordance with claim 9, wherein said selected portion comprises a majority of said thinned semiconductor die.

11. A method in accordance with claim 1, wherein said stress-balancing layer comprises a film.

12. A method in accordance with claim 1, wherein said stress-balancing layer comprises a layer applied to said thinned semiconductor die by one of a chemical vapor deposition (CVD) process, an evaporation process, and an epitaxy process.

13. A method in accordance with claim 1, wherein said stress-balancing layer comprises a layer applied to said thinned semiconductor die by one of LPCVD, APCVD, MOCVD, PECVD, and UHVCVD.

14. A method in accordance with claim 1, wherein said stress-balancing layer comprises a layer applied to said thinned semiconductor die by one of VPE, MBE, and CMOSE.

15. A method in accordance with claim 1, wherein said stress-balancing layer comprises a single homogeneous component.

16. A method in accordance with claim 15, wherein said stress-balancing layer comprises one of a metal, alloy, metalorganic material, photoresist material, and an organic polymer.

17. A method in accordance with claim 1, wherein said stress-balancing layer comprises a heterogeneous composite structure comprising reinforcing particles in a solid matrix material.

18. A method in accordance with claim 17, wherein said reinforcing particles comprise inorganic particles.

19. A method in accordance with claim 17, wherein said reinforcing particles comprise one of a metal, an alloy, glass, and a combination thereof.

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20. A method in accordance with claim 17, wherein said reinforcing particles comprise particles for providing reinforcement in the X-Y plane of said stress-balancing layer.

21. A method in accordance with claim 17, wherein said reinforcing particles comprise particles for providing reinforcement in the X, Y, and Z directions.

22. A method in accordance with claim 17, wherein said matrix material comprises one of silicon dioxide, silicon nitride, and an organic polymeric material.

23. A method in accordance with claim 1, wherein said die comprises one of a DIP, SIP, ZIP, PLCC, SOJ, SIMM, DIMM, LOC, QFP, SOP, TSOP, and a flip-chip.

24. A method in accordance with claim 1, wherein said stress-balancing layer comprises a material markable with indicia.

25. A method in accordance with claim 22, wherein said stress-balancing layer comprises a material markable by optical radiation energy.

26. A method in accordance with claim 22, wherein said stress-balancing layer comprises a polytetrafluoroethylene tape.

27. A method in accordance with claim 23, further comprising exposing a portion of said markable material with optical energy exposing at least a portion of said markable material to one of a Nd:YAG (yttrium aluminum garnet), Nd:YLP (pulsed yttrium fiber laser) or carbon dioxide laser.

28. A method in accordance with claim 1, further comprising:

applying a tape over said stress-balancing layer, said tape comprising a UV-penetrable polyvinyl chloride tape having an acrylic UV-sensitive adhesive disposed thereon; and

exposing a portion of said tape with optical energy exposing at least a portion of said tape to one of a Nd:YAG, Nd-YLP, or carbon dioxide laser.

29. A method in accordance with claim 1, wherein said stress-balancing layer comprises a first sub-layer having high rigidity in the X-direction, and a second sub-layer having high rigidity in the Y-direction.

30. A method in accordance with claim 1, wherein said stress-balancing layer comprises a layer having a coefficient of thermal expansion substantially similar to the coefficient of thermal expansion of said frontside layer.

31. A method in accordance with claim 1, further comprising applying a die-attach adhesive to at least a portion of the surface of said stress-balancing layer.

32. A method in accordance with claim 1, further comprising applying a temporary reinforcement layer over at least a portion of said frontside layer prior to thinning said backside.

33. A method for producing a small Z-dimension non-warped semiconductor die from a semiconductor wafer having a frontside, a backside, and a stress applied thereto by a frontside layer, said method comprising:

reducing a cross-section of said semiconductor die by thinning the backside thereof;
applying a rigid stress-balancing layer to a portion of said thinned backside; and
singulating said wafer into a plurality of non-warped semiconductor dice.

34. A method in accordance with claim 33, wherein said frontside layer comprises a layer applied in a microcircuit fabrication step.

35. A method in accordance with claim 33, wherein said frontside layer comprises a layer of passivation material.

36. A method in accordance with claim 33, wherein said thinning comprises grinding by a grinding apparatus.

37. A method in accordance with claim 33, wherein said thinning comprises a chemical-physical method.

38. A method in accordance with claim 33, wherein said semiconductor die comprises an integrated circuit semiconductor die.

39. A method in accordance with claim 33, wherein said stress-balancing layer comprises a layer substantially covering said thinned backside.

40. A method in accordance with claim 33, wherein said stress-balancing layer comprises a strip covering a selected portion of a row of semiconductor dice on said wafer.

41. A method in accordance with claim 33, wherein said stress-balancing layer comprises a plurality of discrete portions, each said portion covering a selected portion of the thinned backside of a die on said wafer.

42. A method in accordance with claim 41, wherein said selected portion comprises a majority of said thinned die backside.

43. A method in accordance with claim 33, wherein said stress-balancing layer comprises a film.

44. A method in accordance with claim 33, wherein said stress-balancing layer comprises a layer applied to said thinned backside by one of a chemical vapor deposition (CVD) process, an evaporation process, and an epitaxy process.

45. A method in accordance with claim 33, wherein said stress-balancing layer comprises a layer applied to said thinned backside by one of LPCVD, APCVD, MOCVD, PECVD, and UHVCVD.

46. A method in accordance with claim 33, wherein said stress-balancing layer comprises a layer applied to said thinned backside by one of VPE, MBE, and CMOSE.

47. A method in accordance with claim 33, wherein said stress-balancing layer comprises a single homogeneous component.

48. A method in accordance with claim 47, wherein said stress-balancing layer comprises one of a metal, alloy, metalorganic material, photoresist material, and an organic polymer.

49. A method in accordance with claim 33, wherein said stress-balancing layer comprises a heterogeneous composite structure comprising reinforcing particles in a solid matrix material.

50. A method in accordance with claim 49, wherein said reinforcing particles comprise particles of inorganic material.

51. A method in accordance with claim 49, wherein said reinforcing particles comprise one of a metal, an alloy, and glass.

52. A method in accordance with claim 49, wherein said reinforcing particles comprise particles for providing reinforcement in the X-Y plane of said stress-balancing layer.

53. A method in accordance with claim 49, wherein said reinforcing particles comprise particle for providing reinforcement in the X, Y, and Z directions.

54. A method in accordance with claim 49, wherein said matrix material comprises one of silicon dioxide, silicon nitride, and an organic polymeric material.

55. A method in accordance with claim 33, wherein said die comprises one of a DIP, SIP, ZIP, PLCC, SOJ, SIMM, DIMM, LOC, QFP, SOP, TSOP, and a flip-chip.

56. A method in accordance with claim 33, wherein said stress-balancing layer comprises a material markable with indicia.

57. A method in accordance with claim 56, wherein said stress-balancing layer comprises a material markable by optical radiation energy.

58. A method in accordance with claim 56, wherein said stress-balancing layer comprises a polytetrafluoroethylene tape.

59. A method in accordance with claim 56, further comprising exposing a portion of said markable material with optical energy exposing at least a portion of said markable material to one of a Nd:YAG (yttrium aluminum garnet), Nd:YLP (pulsed yttrium fiber laser) or carbon dioxide laser.

60. A method in accordance with claim 1, further comprising applying a tape over said stress-balancing layer, said tape comprising a UV-penetrable polyvinyl chloride tape having an acrylic UV-sensitive adhesive disposed thereon, and exposing a portion of said tape with optical energy exposing at least a portion of said tape to one of a Nd:YAG, Nd-YLP, or carbon dioxide laser.

61. A method in accordance with claim 33, wherein said stress-balancing layer comprises a first sub-layer having high rigidity in the X-direction, and a second sub-layer having high rigidity in the Y-direction.

62. A method in accordance with claim 33, wherein said stress-balancing layer comprises a layer having a coefficient of thermal expansion substantially similar to that of said frontside layer.

63. A method in accordance with claim 33, further comprising applying a die-attach adhesive to at least a portion of the outer surface of said stress-balancing layer.

64. A method in accordance with claim 33, further comprising applying a temporary reinforcement layer over said frontside layer prior to thinning said backside.

65. A method for producing low Z-dimension non-warped semiconductor dice having a frontside, a backside, and a stress applied thereto by a frontside layer, said method comprising:

forming a semiconductor wafer having a frontside, a backside, a plurality of microcircuits on said frontside, and a frontside layer applying stress to said

wafer;

reducing a cross-section of said semiconductor wafer by thinning the backside thereof;

singulating said wafer into a plurality of semiconductor dice; and

applying a rigid stress-balancing layer to said thinned backside under conditions which apply a backside stress generally equivalent to said front-side stress upon restoration to conditions of die use.

66. A method in accordance with claim 65, wherein said frontside layer comprises a layer of passivation material.

67. A method in accordance with claim 65, wherein said stress-balancing layer comprises a layer applied to said backside by one of a chemical vapor deposition (CVD) process, an evaporation process, and an epitaxy process.

68. A method in accordance with claim 65, wherein said stress-balancing layer comprises a layer applied to said backside by one of LPCVD, APCVD, MOCVD, PECVD, and UHVCVD.

69. A method in accordance with claim 65, wherein said stress-balancing layer comprises a layer applied to said backside by one of VPE, MBE, and CMOSE.

70. A method in accordance with claim 65, wherein said stress-balancing layer comprises a single homogeneous component.

71. A method in accordance with claim 70, wherein said stress-balancing layer comprises one of a metal, alloy, metalorganic material, photoresist material, and an organic polymer.

72. A method in accordance with claim 65, wherein said stress-balancing layer comprises a heterogeneous composite structure comprising reinforcing particles in a solid matrix material.

73. A method in accordance with claim 72, wherein said reinforcing particles comprise particles of inorganic material.

74. A method in accordance with claim 72, wherein said reinforcing particles comprise one of a metal, an alloy, and glass.

75. A semiconductor die, comprising:
a semiconductor substrate having a frontside and a backside;
an integrated circuit on a portion of said frontside;
a passivation layer covering a portion of said integrated circuit; and
a stress-balancing layer covering at least a portion of said backside.

76. A semiconductor die in accordance with claim 75, wherein said stress-balancing layer comprises one of a single component layer, a substantially homogeneous mixture of a strong material in a matrix material, a heterogeneous composite of particles of a strong material in a matrix material, and a tape with rigidity in the X-Y plane.

77. A semiconductor die in accordance with claim 75, wherein said stress-balancing layer comprises an adhesive material.

78. A semiconductor die in accordance with claim 75, wherein said stress-balancing layer comprises a layer for laser-marking.

79. A semiconductor die in accordance with claim 75, further comprising an adhesive layer attached to said stress-balancing layer.

80. A non-warp semiconductor die in accordance with claim 79, wherein said adhesive layer comprises a layer of material for laser-marking.

81. A non-warp semiconductor die, comprising:
a semiconductor substrate having a frontside, a backside, and a low ratio of height to a horizontal dimension;
an integrated circuit on said frontside;

a passivation layer covering a portion of said integrated circuit exerting a stress on said substrate frontside;

a stress-balancing layer covering at least a portion of said backside, said stress-balancing layer for balancing a portion of said frontside stress with a generally equivalent backside stress.

82. A non-warp semiconductor die in accordance with claim 81, wherein said stress-balancing layer comprises one of a single component layer, a substantially homogeneous mixture of a strong material in a matrix material, a heterogeneous composite of particles of a strong material in a matrix material, and a tape with rigidity in the X-Y plane.

83. A non-warp semiconductor die in accordance with claim 81, wherein said stress-balancing layer comprises an adhesive material.

84. A non-warp semiconductor die in accordance with claim 83, wherein said stress-balancing layer comprises a layer of material for laser-marking.

85. A non-warp semiconductor die in accordance with claim 81, further comprising an adhesive layer attached to said stress-balancing layer.

86. A non-warp semiconductor die in accordance with claim 85, wherein said adhesive layer for laser-marking.